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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,850	12/22/2003	Shi Chen	1010720-991101	9088

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EXAMINER	
CZEKAJ, DAVID J	
ART UNIT	PAPER NUMBER
2621	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,850	CHEN ET AL.	
	Examiner	Art Unit	
	DAVID CZEKAJ	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 8-13, 17, 24-26, 29, 31-37, 40-41, 45, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (7079583), (hereinafter referred to as "Yoshioka").

Regarding claim 1, Yoshioka discloses an apparatus that relates to digital signal processing (Yoshioka: column 1, lines 10-12). This apparatus comprises "hardware modules configured to execute a decoding process" (Yoshioka: figures 18-19; column 11, lines 45-50, wherein the modules are the VLD, IDCT, IQ, and MC blocks) and "a processing unit that executes a decoding process by sending programmed signals to the modules and responding to interrupts from the components according to a set of programmed instructions" (Yoshioka: column 16, lines 1-9). While Yoshioka fails to explicitly show the bus as claimed, Yoshioka does show communication paths between the various modules (Yoshioka: figure 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a bus architecture in order to allow fast and efficient communication between multiple processing elements.

Regarding claim 2, Yoshioka discloses "a second bus connected to the processing unit at least one module" (Yoshioka: figure 3).

Regarding claim 3, Yoshioka discloses "at least one hardware unit that decodes video according to a video decoding method and at least one audio hardware unit that decodes audio according to an audio decoding method" (Yoshioka: column 13, lines 15-21. The examiner notes the claim language does not limit the hardware units to being different hardware units).

Regarding claim 4, Yoshioka discloses "the hardware modules retrieve audio from the main memory before decoding" (Yoshioka: column 13, lines 15-21).

Regarding claim 5, Yoshioka discloses "a transformation unit that transforms the video data into pixel data" (Yoshioka: column 11, lines 10-17 and 45-50) and "a motion compensation unit that performs interpolations using the pixel data and reference data from the main memory unit" (Yoshioka: column 11, lines 45-50).

Regarding claim 6, Yoshioka discloses "an interface unit that receives compressed MPEG data, wherein the hardware modules comprise a variable length decoder unit" (Yoshioka: figure 3; column 11, lines 45-50).

Regarding claim 8, Yoshioka discloses "executing the decoding process by serially activating certain hardware modules in accordance with a computer program" (Yoshioka: figure 2).

Regarding claim 9, Yoshioka discloses "a first and second processor, wherein the interrupt is programmatically mapped to at least one of the processors" (Yoshioka: figure 3; column 11, lines 5-10; column 16, lines 1-9).

Regarding claim 10, Yoshioka discloses "a local memory unit and an engine for transferring data between the main and local memory units" (Yoshioka: column 13, lines 15-20, wherein the local and main units are the FIFO's and external memory).

Regarding claim 11, Yoshioka discloses "the first processor handles video decoding and display control" (Yoshioka: figure 3). Although not disclosed, it would have been obvious for the second processor to handle the audio decoding (Official Notice). Doing so would have been obvious in order to process the data faster by having multiple processors operating at the same time.

Regarding claim 12, Yoshioka discloses "the main memory unit stores the video and audio data separately" (Yoshioka: column 13, lines 15-20).

Regarding claim 13, Yoshioka discloses "a host unit that receives the video and audio data, parses the data, and stores the data in the main memory unit" (Yoshioka: column 11, lines 28-33; column 12, lines 63-67; column 13, lines 15-20).

Regarding claim 17, Yoshioka discloses "the decoding process comprises variable length decoding, inverse quantization, inverse DCT, and motion compensation that are executed by different hardware modules in response to separate signals" (Yoshioka: figures 18-19; column 11, lines 45-50).

Regarding claim 24, Yoshioka discloses "decoding motion vectors" (Yoshioka: column 11, lines 45-50).

Regarding claim 25, Yoshioka discloses "performing one of inverse quantization" (Yoshioka: column 11, lines 45-50).

Regarding claim 26, Yoshioka discloses "the two-dimensional inverse DCT includes one of row-column decomposition" (Yoshioka: column 11, lines 45-50. The examiner notes that it is well known within the art that a row-column decomposition is performed when using 2-D IDCT).

Regarding claim 29, Yoshioka discloses "the apparatus is integrated as a system-on-chip system" (Yoshioka: figures 3-4).

Regarding claims 31 and 36, although not disclosed, it would have been obvious to have modules for decrypting input data (Official Notice). Doing so would have been obvious in order to correctly read encrypted data.

Regarding claim 32, note the examiners rejection for claim 1.

Regarding claim 33, note the examiners rejection for claims 1 and 23.

Regarding claim 34, note the examiners rejection for claims 3 and 13.

Regarding claim 35, note the examiners rejection for claims 3 and 12-13.

Regarding claim 37, Yoshioka discloses "extracting header information, converting the macroblock into pixel data, and generating a reconstructed image based on the pixel data by using motion compensation, wherein a motion compensation module is reprogrammable for each block" (Yoshioka: column 11, lines 25-50).

Regarding claim 40, note the examiners rejection for claim 25.

Regarding claim 41, Yoshioka discloses "the modules process different blocks simultaneously" (Yoshioka: column 11, lines 1-10, wherein the simultaneous processing is the parallel processing).

Regarding claim 45, note the examiners rejection for claim 31.

Regarding claim 50, note the examiners rejection for claim 1.

3. Claims 7, 14, 18-19, 22-23, 27-28, 30, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (7079583), (hereinafter referred to as "Yoshioka") in view of Alvarez et al. (2003/0185298), (hereinafter referred to as "Alvarez").

Regarding claim 7, note the examiners rejection for claim 1, and in addition, claim 7 differs from claim 1 in that claim 7 further requires triggering an interrupt upon finding a startcode. Alvarez teaches that prior art encoders/decoders are inefficient and not cost-effective at solving certain problems (Alvarez: paragraph 0006). To help alleviate this problem, Alvarez discloses "the VLD sends an interrupt upon finding a startcode which triggers the decoding method" (Alvarez: paragraphs 0030, 0031, 0033, wherein the interrupt is the notification, the startcode is the command detected by the core processor to indicate the decoding process has started). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the decoding scheme taught by Alvarez in order to provide a cost-effective solution of eliminating prior art problems.

Regarding claim 14, Alvarez discloses "an assist hardware unit that receives interrupts generated by the modules and forwards the interrupts to the processing unit" (Alvarez: figures 1 and 4; paragraphs 0032-0033).

Regarding claim 18, Yoshioka in view of Alvarez disclose "determining a decoding status, evaluating header parameters, and checking for errors" (Yoshioka: column 11, lines 5-11; Alvarez: paragraph 0033, wherein the task completion indicates the decoding status).

Regarding claim 19, Alvarez discloses "the processing unit reads registers in different hardware modules, the registers indicating a current process state and presence of any errors" (Alvarez: paragraph 0033, wherein the register is the status register).

Regarding claim 22, Alvarez discloses "an interrupt from a hardware module in charge of motion compensation indicates that the decoding process is completed for a portion of an image" (Alvarez: paragraphs 0032-0033).

Regarding claim 23, Alvarez discloses "sending signals to the modules in an order dictated by a program" (Alvarez: paragraph 0033, wherein the signals are the polling signals which are sent as indicated by a program). Although not disclosed, it would have been obvious to change the decoding process by the computer program (Official Notice). Doing so would have been obvious in order to provide a customizable system to a user.

Regarding claim 27, Alvarez discloses "a buffer associated with each of the modules" (Alvarez: paragraph 0040).

Regarding claim 28, Alvarez discloses " a memory unit" (Alvarez: figure 2. The examiner notes that it is well known for a memory unit to be divided into cells according to a luminance and chrominance indicator).

Regarding claim 30, Alvarez discloses "interrupt signals generated by different hardware modules as each of the modules completes its task" (Alvarez: paragraph 0033, wherein the signals are generated which update the status in the status register).

Regarding claim 38, note the examiners rejection for claim 28.

4. Claims 15-16, 20-21, 39, 42-44, and 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (7079583), (hereinafter referred to as "Yoshioka") in view of Alvarez et al. (2003/0185298), (hereinafter referred to as "Alvarez") in further view of Deiss (5802063).

Regarding claim 15, note the examiners rejection for claim 7, and in addition, claim 15 differs from claim 7 in that claim 15 further requires an arbitration scheme. Deiss teaches that storing an arbitration scheme for the modules helps determine which data gets processed first (Deiss: column 12, lines 17-47, wherein the arbitration scheme is the priority scheme). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the arbitration scheme taught by Deiss in order to better help the throughput of the system by assigning priorities to different pieces of data.

Regarding claim 16, Deiss discloses "the arbitration scheme comprises prioritization of video transfers over audio transfers" (Deiss: column 12, lines 34-36).

Regarding claim 20, Deiss discloses "generate correct data from incorrect data" (Deiss: column 3, lines 7-24, wherein the error correcting coding corrects the data).

Regarding claim 21, Deiss discloses "purging the error from the decoding process upon determining the error is incorrigible" (Deiss: column 3, lines 7-24).

Regarding claim 39, note the examiners rejection for claim 16.

Regarding claims 42-44, note the examiners rejection for claims 18, 20, and 21.

Regarding claim 46, note the examiners rejection for claim 15.

Regarding claim 47, note the examiners rejection for claim 17.

Regarding claim 48, Yoshioka discloses "the first module processes another block while the second module is processing the block" (Yoshioka: column 11, lines 1-10, wherein the processing is the sequential processing).

Regarding claim 49, Yoshioka discloses "decompression of the macroblock" (Yoshioka: column 11, lines 45-50).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US-6847656	01-2005	Wu et al.
US-6792047	09-2004	Bixby et al.
US-6748020	06-2004	Eifrig et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID CZEKAJ whose telephone number is (571)272-7327. The examiner can normally be reached on Mon-Thurs and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dave Czekaj/
Primary Examiner, Art Unit 2621
TC 2600